REMARKS

In the Office Action dated September 16, 2004, claims 1–21 were considered. Claims 1, 7, 13, and 21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 1–9, 11–17, and 19–21 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,141,769 to Petivan et al. ("Petivan"). Claims 10 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Petivan.

Applicants hereby amend claims 1–3, 5–7, 10–15 and 19–21 without any intention of disclaiming any equivalents thereof. Applicants also add new claims 22–24. Support for the amendments to claims 1–3, 5–7, 10–15, and 19–21, as well as new claims 22–24 may be found in the specification, for example at pages 2–3, 7–8, 21–23, 29–31, and 33. Support for the amendments to independent claims 1, 13, and 21, and new claims 22–24 may also be found in the drawings, for example in Figures 2, 6, and 8, and in the claims as originally-filed.

Applicants respectfully submit that no new matter is entered by the present amendments to claims 1–3, 5–7, 10–15, and 19–21, and new claims 22–24. Upon entry of this paper, claims 1–24 will be pending in this application. Reconsideration is respectfully requested.

Rejection of Claims 1, 7, 13, and 21 Under 35 U.S.C. §112

Claims 1, 7, 13, and 21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention. Particularly, the Examiner objected to the term "substantially similar." The present amendments to claims 1, 7, 13, and 21 moot this ground of rejection.

Rejection of Claims 1–9, 11–17, and 19–21 Under 35 U.S.C. §102(e)

Claims 1–9, 11–17, and 19–21 were rejected under 35 U.S.C. §102(e) as being anticipated by Petivan.

Generally, Petivan teaches a fault tolerant computer system where information is transferred among three system modules in order to defect possible system faults. (Abstract; Col. 3, lines 53-60.) Specifically, Petivan discloses that:

> in order to write data to an I/O device during normal synchronous

> system operation, all three processors synchronously direct a write request to the I/O controller local to the module that controls the target I/O device. The information to be written is actually provided to the I/O controller interface by the processor local to the target I/O device. Thus, although all three processors provide to their respective local buses the same write information, only the processor local to the target I/O device presents the information to the I/O controller interface. The subject I/O controller responds by causing the write information to be written to the target I/O device.

(Col. 5, lines 7-17. Emphasis added)

Further, "[t]he transaction information incident to the write transaction is subject to pairwise comparisons. If an error is detected, then each of the three processors runs a diagnostic program to evaluate possible causes of the error." (Col. 5, lines 21-24.)

In sum, Petivan discloses accessing a target I/O device only from the processor local to that I/O device, via an I/O controller also local to that same I/O device. Information from another processor, such as a processor from a remote module, is incident to the transaction, and is only used for pairwise comparisons. Thus, in Petivan, information written to the target I/O device can only originate from the processor local to that target I/O device, and Petivan prohibits providing information from a processor to a target I/O device local to any other processor.

Amended Independent Claim 1

Applicants' amended independent claim 1 recites, in part,

> (b) a first Central Processing Unit, (CPU), in electrical communication with the communications link and capable of transmitting a first information stream;
> (c) a second CPU, in electrical communication with the communications link and capable of transmitting a second information stream;
> (d) a first Input/Output (I/O) subsystem, in electrical communication with the first CPU and with the communications link, configured to compare the first information stream and the second information stream; and
> (e) a first local mass storage device in electrical communication with the first I/O subsystem,
> wherein the first I/O subsystem selectively accesses the first local mass storage device in response to a comparison of the first and second information streams.

Petivan fails to teach or suggest these limitations of Applicants' amended independent claim 1. Specifically, Petivan does not teach or suggest at least a system "wherein the first I/O subsystem selectively accesses the first local mass storage device in response to a comparison of the first and second information streams." Instead, as described above, Petivan teaches that only the processor local to the target I/O device presents the information to the local I/O controller. This is different from the Applicants claimed invention where each I/O subsystem compares at least two information streams received from separate CPUs and selectively accesses an I/O device in response to the results of the comparison.

Accordingly, for at least this reason, Applicants respectfully submit that amended independent claim 1 is patentable over Petivan.

Amended Independent Claim 13

Applicants' amended independent claim 13 recites, in part,

> establishing communication between a first Central Processing Unit (CPU) and a first local mass storage device capable of transmitting a first information stream;
> (b) establishing communication between a second CPU and a second local mass storage device capable of transmitting a second information stream;
> (c) providing a first Input/Output (I/O) subsystem, in communication with the first CPU and the first local mass storage device, configured to compare the first information stream and the second information stream; and
> (d) selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information streams.

As discussed above with respect to Applicants' amended independent claim 1, Petivan at least fails to teach or suggest "selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information streams."

Accordingly, for at least this reason, Applicants respectfully submit that amended independent claim 13 is also patentable over Petivan.

Amended Independent Claim 21

Likewise, Applicants' amended independent claim 21 recites, in part,

> (d) means for selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information streams.

However, as discussed above with respect to Applicants' amended independent claims 1 and 13, Petivan fails to teach or suggest at least a means for selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information streams.

Accordingly, for at least these reasons, Applicants respectfully submit that amended independent claim 21 is also patentable over Petivan.

New Independent Claims 23 and 24

Likewise, Applicants' new independent claims 23 and 24 recite elements similar to those discussed above.

Accordingly, for at least these reasons, Applicants respectfully submit that new independent claims 23 and 24 are also patentable over Petivan.

Dependent Claims 2–12, 14–20, and 22

Because claims 2–12 14–20, and 22 depend directly from one of amended independent claims 1 or 13, Applicants submit that these claims are also patentable over Petivan. Likewise, Applicants submit that the rejections to dependent claims 10 and 18 under 35 U.S.C. §103(a) as being anticipated by Petivan are moot in light of the amendments to independent claims 1 and 13.

Accordingly, Applicants respectfully request that the rejection of claims 1–9, 11–17, and 19–21 under 35 U.S.C. §102(e), and the rejection of claims 10 and 18 under 35 U.S.C. §103(a), all as being anticipated by Petivan, be reconsidered and withdrawn.

CONCLUSION

Applicants believe the above amendments and remarks to be fully responsive to all the grounds of rejection raised in the Office Action. Applicants request that the Examiner reconsider the application and claims 1–24 in light of the foregoing Amendment and Response, and respectfully submit that the pending claims are in condition for allowance. Accordingly, Applicants request withdrawal of all grounds of rejection, and allowance of claims 1–24 in due course.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Regards,

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